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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,185	09/24/2002	Johni Chan	73543	6299

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/065,285	Applicant(s) ~~BRAUN ET AL.~~ Chan, Johni	
	Examiner Khanh Dang	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 23-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of group II, claims 23-25 readable thereon, in the reply filed on 4/28/2005 is acknowledged. Because Applicants cancelled the non-elected claims 1-22, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

Claims 23-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 23-25 are directed to an apparatus. However, the essential structural cooperative relationships between the "peer coupling," "control and status register," "sequencer," "register interface," and "arbiter" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01.

With regard to claim 25, the language "the register interface includes an arbiter state" is unclear and cannot be ascertained. It is unclear what may be the relationship between the words "interface" and "state."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Pincus et al. (Pincus, 6,282,583).

As broadly drafted, these claims do not define any structure that differs from Pincus et al. (Pincus, 6,282,583).

With regard to claim 23, Pincus discloses an apparatus for controlling access to a bus, comprising: a peer coupling to communicate state information (it is clear from Pincus that each CPU 40, for example, are coupled to another CPU 40, and coupled to the at least multiple registers provided by register arrays 88 to communicate state information); a control and status register (multiple CPU registers are provided in CPU register array 88, including the CPU barrier control and status register (suitably one per node, with one bit per CPU) which may be used to indicate and determine when a CPU is at a barrier state, a hold mask enable control and status register which allows individual or multiple CPUs on a node to be placed in a "HOLD" condition (i.e. suspended from using the node bus) when both a hold mask enable bit and a CPU barrier bit for the corresponding CPU are set, and a configuration mask control and status register which allows software to configure CPUs into or out of the node. Each CPU is represented by a bit in the configuration mask control and status register whereby the currently available CPUs in the configuration register can define the "next"

CPU. The node arbitration control and status register contains the value associated with the CPU on the node having highest round robin priority within a node. A software interrupt control and status register (also included in array 88) allows individual or multiple CPUs to be interrupted by a write to the register (or returns status when read). The CPU registers may be accessed locally by the processing elements on the node without any access to the memory system.; and a sequencer (in Pincus, sequencer 24 includes an array of CPU (i.e. processor) registers (included in multiple registers provided by register arrays 88) that are manipulated by the processing elements on the bus based on whether they are requesting, using or releasing data bus 16. Each processor reads the CPU registers in sequencer 24 prior to accessing memory 14 to determine if the processor is allowed access. When access to the bus is given, the processor transfers data to memory 14 and then disables a register bit in a register of sequencer 24. Sequencer 24 then enables the processor with the next highest priority) to transition the state of the apparatus.

With regard to claims 24 and 25, in Pincus, either the node arbitration control and status register (provided by register array 88 and connected to arbiter 52/144) or the arbitration control register 300 is readable as a register interface coupled to an arbiter. The node arbitration control and status register contains the value associated with the CPU on the node having highest round robin priority within a node. The apparatus as claimed in claim 23, further comprising: a register interface coupled with an arbiter. See also Figs. 12(a, b) and description thereof.

U.S. Patent Nos. 4,630,265 to Sexton, 5,377,332 to Entwistle et al., and US 2003/0192000 to Vail et al. are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner